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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,956	10/31/2005	Wolfgang Clemens	411000-137	8177

27162 7590 12/13/2007

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EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
12/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,956	CLEMENS ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/07 & 5/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/08/2007 has been entered. An action on the RCE follows.

Information Disclosure Statement

The information disclosure statement filed 05/24/2007 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 2 and 3-15 and 17-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Amended claim 2 recites "wherein the at least one active organic electrical component and the at least one passive organic electrical component each include an organic layer forming a portion of that component and wherein the organic layer of each component is interconnected to and forms a corresponding conductive track on the circuit board surface for interconnection with at least one other electrical device on the circuit board surface to form an integrated preassembled circuit assembly" (emphasis added). Whereas the specification states that organic components may have organic layers, the specification is silent about the organic layer of each component forming a conductive track for interconnection with other devices. Please clarify.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 3-15 and 17-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 22 recite "the organic electronic component at least one electrode layer". This is not clear as to what it means. Note that in claim 1, the word "having" has been specifically deleted as follows "the organic electronic component ~~having~~ at least one electrode layer". For the purpose of this office action, it will be assumed that the word "having" was inadvertently struck off in claim 1 and inadvertently missed in claim 22. A correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-11, 14-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US 2001/0046081) hereinafter Hayashi.

Regarding claim 1, Hayashi (refer to Figures 1A-1F, 2A-2E, 3C, 3D and 4A-4F) teaches a circuit board arrangement for an organic electronic device, comprising:

a preassembled circuit board (page 6, para 0117 and page 8, para 0148) assembly forming a circuit comprising a printed circuit board on which are a plurality of interconnected electrical conductors (page 8, para 0149) and at least one active organic electronic component (page 8, para 0151, 1st sentence);

the circuit board having a surface on which are disposed a plurality (page 8, para 0148, 3rd sentence) of electrically interconnected electrical devices including said at least one active organic component and said interconnected conductors;

at least one of the interconnected electrical devices comprising the at least one active organic (page 8, para 0147) electronic component (with source electrode 33, as shown in Figure 4C), the at least one active organic electronic component including at least one electrode layer (page 8, para 0147) electrically integrated on the circuit board surface with at least one of the interconnected devices to form at least a portion of an electrical circuit; the organic electronic component at least one electrode layer (31, see Figure 4c) forming a portion of the active organic electronic component;

the at least one electrode layer of the integrated active organic electronic component for forming a conductive track layer (16b of Figures 3C or 3D) on the surface and forming a connection to an inorganic (page 8, para 0151, first sentence) semiconductor electrical component (page 8, para 148, 1st sentence and para 149).

Whereas Hayashi teaches that the active organic electronic component and an inorganic semiconductor electrical component may be interconnected (page 8, para 148, 1st sentence and para 149), Hayashi does not categorically disclose that the one electrode layer of the integrated active organic electronic component for forming a conductive track layer on the surface is specifically "for connection to an inorganic semiconductor electrical component". However, since the electrode layer of the integrated active organic electronic component is suitable for interconnection to any of the devices on the circuit board (page 8, para 0149), it would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the conductive track layer on the surface is for connection to an inorganic semiconductor electrical component. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of achieving a specific interconnection scheme between components as may be required by an application specific design.

Regarding claim 22, Hayashi (refer to Figures 1A-1F, 2A-2E, 3C, 3D and 4A-4F) teaches a circuit board arrangement for an organic electronic device, comprising:

a preassembled circuit board (page 6, para 0117 and page 8, para 0148) assembly forming a circuit comprising a printed circuit board on which are a plurality of interconnected electrical conductors (page 8, para 0149) and at least one active organic electronic component (page 8, para 0151, 1st sentence);

the circuit board having a surface on which are disposed a plurality (page 8, para 0148, 3rd sentence) of electrically interconnected electrical devices including said at least one active organic component and said interconnected conductors;

at least one of the interconnected electrical devices comprising the at least one active organic (page 8, para 0147) electronic component (with source electrode 33, as shown in Figure 4C), including at least one functional layer (page 8, para 0147) electrically integrated on the circuit board surface with at least one of the interconnected devices to form at least a portion of an electrical circuit; the organic electronic component at least one functional layer (31, see Figure 4c) forming a portion of the active organic electronic component;

the at least one functional layer of the integrated active organic electronic component for forming a conductive track layer (16b of Figures 3C or 3D) on the surface and forming a connection to an inorganic (page 8, para 0151, first sentence) semiconductor electrical component (page 8, para 148, 1st sentence and para 149).

Whereas Hayashi teaches that the active organic electronic component and an inorganic semiconductor electrical component may be interconnected (page 8, para 148, 1st sentence and para 149), Hayashi does not categorically disclose that the one functional layer of the integrated active organic electronic component for forming a conductive track layer on the surface is specifically "for connection to an inorganic semiconductor electrical component". However, since the functional layer of the integrated active organic electronic component is suitable for interconnection to any of

the devices on the circuit board (page 8, para 0149), it would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the conductive track layer on the surface is for connection to an inorganic semiconductor electrical component. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of achieving a specific interconnection scheme between components as may be required by an application specific design.

It is to be noted that claims 1 and 22 are product claims but recite a "preassembled circuit board" (emphasis added), which is directed to a method as it indicates a sequence of assembly steps of the circuit board. Therefore, the limitation "preassembled" in the above claimsamounts to a product by process limitation(s), which will not be given patentable weight. *"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.*

Regarding claim 2, Hayashi teaches a circuit board arrangement for an electronic device comprising:

a circuit board (page 6, para 0117 and page 8, para 0148) defining a surface; and

at least one active organic (page 8, para 0147) electrical component (with source electrode 33, as shown in Figure 4C) and at least one passive organic electrical component (page 8, para 0144, 1st sentence and para 0149, 2nd last sentence) integrated to form at least a portion of an electrical circuit on the surface wherein the at least one active organic electrical component and the at least one passive organic electrical component each include an organic layer forming a portion of that component and wherein the organic layer of each component is interconnected to and forms a corresponding conductive track on the circuit board surface for interconnection with at least one other electrical device on the circuit board surface to form an integrated preassembled circuit assembly.

However, Hayashi does not specifically state that the at least one passive component also includes "an organic layer" forming a portion of that component and the organic layer is "interconnected to and forms a corresponding conductive track". However, Hayashi does teach that in general, electrodes of devices (page 7, paras 0135-0136 and page 8, para 0147, 2nd sentence) or interconnection wiring page 8, para 0149, 2nd last sentence) may be made of an organic layer. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the display comprises at least one passive organic electrical component that includes "an organic layer" forming a portion of that component and wherein the organic layer is

"interconnected to and forms a corresponding conductive track" on the circuit board surface for interconnection with at least one other electrical device on the circuit board surface to form an integrated preassembled circuit assembly. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of increasing the organic material content of the device for process compatibility/cost savings and for a thinner, more flexible final assembly (page 2, para 0023, last 3 sentences).

Regarding claim 3, Hayashi teaches that the at least one active electrical component is an organic transistor (page 8, para 0147 or para 151, 1st sentence), and/or the passive organic (as modified above for claim 2) component is a capacitor (page 8, para 0144, 1st sentence).

Regarding claim 4, Hayashi teaches that the device includes a power supply (page 8, para 0144, 1st sentence) integrated with the electrical circuit on the surface (page 8, para 0145, 1st sentence).

Regarding claim 5, Hayashi teaches that the substrate wherein an input element (page 6, para 0112 and para 0113) and/or an output element (page 6, para 0110)) is integrated on the substrate.

Regarding claim 6, Hayashi teaches that the electrically conductive lines or conducting contacts are on the surface using structured conductive layers, and/or conductive

adhesives and which may form electrodes for the electrical components (page 8, para 0147, 1st and 2nd sentence).

Regarding claim 7, Hayashi teaches an visualization element and/or a display (Col. 4, lines 52 and 55) is integrated on the substrate.

Regarding claim 9, Hayashi teaches that a driver circuit associated with the display is electrically integrated on the surface with the circuit (page 8, para 0146).

Regarding claim 10, Hayashi teaches that the driver circuit comprises at least one organic field-effect transistor (page 8, para 0151, 1st sentence).

Regarding claim 14, Hayashi teaches that a driver electronics is included and comprises at least one organic field-effect transistor (page 8, para 0151, 1st sentence).

Regarding claims 11 and 15, the claims merely recite use language. The device of Hayashi, which is a display device, is capable of being used at least as a price marker.

Regarding claims 17-18, 20 and 21, Hayashi teaches that the circuit board arrangement may include a further arrangement coupled to the circuit for operating the circuit as a display device (page 4, para 0081), but does not specifically state that the display is specifically configured as a price marker. However, the use of displays to display information (including price) and hence its use as a price marker is well known in the

art. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the further arrangement coupled to the circuit is for operating the circuit as a price marker. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of utilizing a cost effective price marker that is less prone to tampering by customers and/or which can potentially reduce labor costs associated with pricing updates.

Claims 8, 12, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (US 2001/0046081) hereinafter Hayashi, in view of Antoniadis (US 6,366,017), hereinafter Antoniadis.

Regarding claim 8, Hayashi teaches that the display comprises electrochromic material (page 6, para 0125) or liquid crystalline elements (page 6, para 0124, 2nd sentence), However, Hayashi does not teach that the display comprises organic light-emitting diodes. Antoniadis US (6,366,017) teaches the use the use of organic light-emitting diodes in displays (Col. 1, lines 10-15). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the display comprises electrochromic material, liquid crystalline elements and/or organic light-emitting diodes. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of optimizing display design taking advantage of the good resolution resulting from liquid crystal elements, the ability to use non-transparent

substrates with organic light-emitting diode, and the reduced power consumption advantage of electrochromic materials.

Regarding claim 12, Hayashi teaches that a driver circuit associated with the display is electrically integrated on the surface with the display (page 8, para 0146).

Regarding claim 13, Hayashi teaches that a driver electronics is included and comprises at least one organic field-effect transistor coupled to the circuit (page 8, para 0151, 1st sentence).

Regarding claim 19, Hayashi teaches that the circuit board arrangement may include a further arrangement coupled to the circuit for operating the circuit as a display device (page 4, para 0081), but does not specifically state that the display is specifically configured as a price marker. However, the use of displays to display information (including price) and hence its use as a price marker is well known in the art. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Hayashi so that the further arrangement coupled to the circuit is for operating the circuit as a price marker. The ordinary artisan would have been motivated to modify Hayashi for at least the purpose of utilizing a cost effective price marker that is less prone to tampering by customers and/or which can potentially reduce labor costs associated with pricing updates.

Response to Arguments

Applicant's arguments filed 08/08/2007 have been fully considered but they are not persuasive.

On page 11, applicant argues regarding Fig. 3D that it shows a semiconductor chip that is "not organic" and the wiring pattern is "not shown to be part of an organic component electrode layer". Applicant appears to allege that the Hayashi reference does not show an active organic electronic component. However, as mentioned in the rejection of claim 1, the active organic electronic component is described on page 8, para 0151, 1st sentence and further figures 4A-4F show that wiring pattern is part of an organic component electrode layer (see rejection of claim 1 for more details).

On page 12, applicant argues that "None of these embodiments disclose an inorganic device in the assemblies described and here to there is no basis in this disclosure to assume the construction of the various elements to which the patent is silent". Applicant concludes that "No inorganic device is disclosed in these sections". This argument is not persuasive. Referring to rejection of claim 1 and 22, the part of the reference that specifically shows an inorganic device, such as a silicon device, is quoted as (page 8, para 0151, first sentence).

On page 13, applicant argues that "this latter organic conductive material is not discloses as forming an electrode of an organic active component as claimed". However, the applicant does not clarify which claim is being referred to. It will be assumed that this with reference to amended claim 2. Applicant's above arguments with respect to amended claim 2 have been considered but are moot in view of the new ground(s) of rejection.

On page 14, applicant alleges that "At best, there is only disclosed unrelated aspects of different structures in different embodiments. This amounts to a proscribed invitation to experiment with mere possibilities". This argument is not persuasive. The rejections refer to Figures 1A-1F, 2A-2E, 3C, 3D and 4A-4F and associated descriptions, and all of these figures are depicting various aspects of the same embodiment with minor variations (refer to description of Figures on page 3, para 0044-0047). . For example, Fig. 1E shows that the display layer (12) and electric layer (14). Figures 2A-2E, 3C, 3D and 4A-4F provide further details of the variations of display layer (12) and electric layer (14) of Fig. 1A. Clearly, any of these variations can be used in the structure of say Figures 1E. Figures 2A-2B are focused on providing details of the display layer (12), seepage 3, para 0045, including electrodes (16). Figures 3A-3D are focused on further details of the electrodes (16). Figures 4A-4F are focused on providing details/variations of the electric layer (14), see page 3, para 0047, including Figure 4C which shows further details with an example of the structure of a transistor used for forming a circuit in an electric layer (page 8, para 0147, 1st sentence). This is a reasonable method to

show various possible structures and does not invite "experiment with mere possibilities".

On page 14, applicant specifically asks the examiner to "point out where an electrode of an organic device is expressly disclosed that forms a conductive track layer on the surface of a PCB for connection to an inorganic semiconductor electrical component", as claimed in amended claim 1. This arguments has been considered but is moot in view of the new ground(s) of rejection for amended claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AKA

Date: December 10, 2007

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